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FORM PTO-1390 (REV. 5-93)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER 52433/545
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		U.S. APPLICATION NO (If known, see 37 CFR 1.5) 09/254119

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATES CLAIMED
PCT/JP97/02987	(27.08.97) 27 August 1997	(27.08.96) 27 August 1996

TITLE OF INVENTION
SEMICONDUCTOR DEVICE PROVIDED WITH LOW MELTING POINT METAL BUMPS AND PROCESS FOR PRODUCING SAME

APPLICANT(S) FOR DO/EO/US
TATSUMI, Kohei; SHIMOKAWA, Kenji and HASHINO, Eiji

Applicants herewith submit to the United States Designated/Elected Office (DO/EO/US) the following items and other information

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☒ A translation of the International Application into English (35 U.S C 371(c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A **FIRST** preliminary amendment.
    ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information: International Search Report and PCT/RO/101.

EXPRESS NO . EL303285061US
65269

U.S. APPLICATION NO if known, see 37 C.F.R 1.5	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
	PCT/JP97/02987	52433/545

17. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
Basic National Fee (37 CFR 1.492(a)(1)-(5)): Search Report has been prepared by the EPO or JPO $840.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) $670.00		
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) $760.00		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO $970.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) $96.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 840.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

Claims	Number Filed	Number Extra	Rate		
Total Claims	15 - 20 =	0	X $18.00	$	
Independent Claims	3 - 3 =	0	X $78.00	$	
Multiple dependent claim(s) (if applicable)			+ $260 00	$	
TOTAL OF ABOVE CALCULATIONS =				$840.00	
Reduction by 1/2 for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 CFR 1.9, 1.27, 1.28).				$	
SUBTOTAL =				$	
Processing fee of $130.00 for furnishing the English translation later the ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$	
TOTAL NATIONAL FEE =				$840.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property +				$	
TOTAL FEES ENCLOSED =				$840.00	
				Amount to be. refunded	$
				charged	$

a. ☐ A check in the amount of $_____ to cover the above fees is enclosed.

b. ☒ Please charge my Deposit Account No. 11-0600 in the amount of **$840.00** to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 11-0600. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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Edward W. Greason
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Feb 20, 1999
DATE

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

PRELIMINARY AMENDMENT			Docket Number 52433/545	
International Application Number	International Filing Date	U S Filing Date	Examiner	Art Unit
PCT/JP97/02987	August 27, 1997	Herewith		
Invention Title: SEMICONDUCTOR DEVICE PROVIDED WITH LOW MELTING POINT METAL BUMPS AND PROCESS FOR PRODUCING SAME			Inventor(s): TATSUMI, Kohei et al.	

Assistant Commissioner for Patents
Washington D.C. 20231
Box PCT

SIR:

Please amend the above-referenced patent application as follows:

In the Claims:

In claim 3, lines 1 and 2, delete "or 2";

In claim 9, line 1, delete "or 8";

In claim 13, lines 1 and 2, delete "any one of claims 10 to 12" and substitute --claim 10--;

In claim 14, line 2, delete "any one of claims 7 to 9" and substitute --claim 7--;

In claim 15, lines 2, delete "any one of claims 10 to 13" and substitute --claim 10--;

Remarks

The specification has been amended in order to eliminate multiple dependent claims.

An early indication of allowable subject matter is respectfully requested.

The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 11-0600. Duplicate copies of this sheet are enclosed herewith.

Dated: Feb 25 1999

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65293

Express Mail No. EL303285061US

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

PRELIMINARY AMENDMENT			Docket Number 52433/545	
International Application Number	International Filing Date	U S Filing Date	Examiner	Art Unit
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Dated: Feb 25, 1999

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Express Mail No. EL303285061US

DESCRIPTION

SEMICONDUCTOR DEVICE PROVIDED WITH LOW MELTING POINT METAL BUMPS AND PROCESS FOR PRODUCING SAME

Technical Field

The present invention relates to a semiconductor device provided with low melting point metal bumps and a process for producing the same.

Background Art

Semiconductor devices have currently been used widely in various fields. The semiconductor devices are usually used by mounting them on substrates. The mounting methods include bonding methods such as tape automated bonding (TAB), wire bonding and flip chip bonding.

The TAB and wire bonding are technologies by which a semiconductor device is mounted on a substrate through leads. The leads are arranged in one row per peripheral side of the semiconductor device. The technologies are, therefore, not suited to high density mounting of the semiconductor devices. In contrast to the technologies mentioned above, flip chip bonding is a technology by which the electrodes of a semiconductor device are directly connected to the electrode terminals on the substrate through a bonding metal. Since the electrodes of the semiconductor device can be provided in a lattice-like form on the entire surface, the technology is suited to high density mounting. Various solders are generally used as bonding metal in flip chip bonding because the bonding is conducted by melting at low temperature.

In flip chip bonding, semiconductor devices provided with low melting point metal bumps for bonding placed on electrodes are used, and the semiconductor devices are connected to the electrode terminals of substrates by a reflowing procedure by which the bumps are melted and solidified again.

In general, the bumps are formed by vapor deposition or plating. However, such bump formation methods must all repeat complicated treatments steps using a mask. Moreover, in the method of forming the bumps by vapor deposition, a bump material is deposited on portions where the bumps are not to be formed, and the deposition amount thereon is very large. The method is, therefore, not a preferred one in view of the cost and efficiency. Moreover, wet plating such as electroplating or electroless plating fouls wafers and causes an environmental problem, and countermeasures against such problems are indispensable. As illustrated above, conventional methods for forming the bumps are relatively costly, and practical use of the methods is restricted.

There is a stud bump procedure as a method for forming bumps other than vapor deposition and plating. Since bumps are formed one by one in the procedure, the production efficiency is low, and in addition the bump amount tends to vary among the bumps. Accordingly, securing uniformity in bonding the semiconductor devices and the substrates is difficult.

Disclosure of the Invention

An object of the present invention is to provide a semiconductor device provided with low melting point metal bumps of high quality and capable of being mounted on a substrate by flip chip bonding, and a process for producing the same.

The semiconductor device of the present invention comprises electrodes formed on a semiconductor chip, and is provided with bumps each consisting of a low melting point metal ball which is spherically formed and has a given size, and adhesive bonded to the electrodes.

The low melting point metal balls are preferably adhesive bonded to the respective electrodes with a flux.

The electrodes on the semiconductor chip are preferably formed from an electrode material of Cu or a Cu alloy, Al or an Al alloy, or Au or a Au alloy.

When the electrode material is Al or an Al alloy, at least one layer of a metal or a metal alloy having a melting point higher than the electrode material is preferably laminated to the layer formed from the electrode material.

The laminated layers are preferably formed from a metal selected from Ti, W, Ni, Cr, Au, Pd, Cu, Pt, Ag, Sn and Pb, or an alloy of these metals.

It is preferred that, of the layers laminated to the electrode material layer, the layer contacted with the electrode material layer be formed from Ti, W, Ni, Cr, Pd, Cu or Pt, or an alloy of these metals, and that the layer contacted with the low melting point metal ball be formed from Ni, Au, Pd, Cu, Pt, Ag, Sn or Pb, or an alloy of these metals.

The process for producing a semiconductor device according to the present invention is a process for producing a semiconductor device having electrodes formed on a semiconductor chip, and provided with bumps which consist of low melting point metal balls each being formed spherically and having a given size, and which are adhesive bonded to the respective electrodes, and is characterized by the low melting point metal balls being adhesive bonded and fixed to the respective electrodes with a flux.

The flux is preferably applied to the electrodes.

On another aspect of the present invention, the process for producing a semiconductor device according to the present invention is a process for producing a semiconductor device provided with low melting point metal bumps on the electrodes on a semiconductor chip, the process comprising the steps of:

adhesive bonding low melting point metal balls each being spherically formed and having a given size to the respective electrodes, and

reflowing the low melting point metal balls.

The low melting point metal balls are preferably adhesive bonded to the respective electrodes with a flux. The flux is preferably applied to the electrodes.

Brief Description of the Drawings

Fig. 1 is a perspective view illustrating a semiconductor device of the present invention.

Fig. 2 is a view illustrating an electrode in the semiconductor device of the present invention.

Fig. 3 is a view illustrating a semispherical bump of the semiconductor device of the present invention which bump is formed by reflowing a low melting point metal ball.

Figs. 4A to 4D are views illustrating a process for producing the semiconductor device of the present invention.

Fig. 5 is a view illustrating a bump of a solder ball directly formed on a chip electrode of a single material.

Figs. 6A and 6B are views illustrating a preferred method for adhesive bonding low melting point metal balls to the respective electrodes.

Best Mode for Carrying Out the Invention

Fig. 1 shows a semiconductor device 1 of the present invention. The semiconductor device 1 is provided with low melting point metal ball bumps 3 adhesive bonded onto the electrodes (not shown) formed on a surface of a semiconductor chip 2.

The low melting metal balls 3 can be formed from one of the various solders used for mounting a semiconductor device on a substrate. Examples of the solders include solders of Sn alloys such as a Sn-Pb alloy and a Sn-Ag alloy and solders of Pb alloys such as a Pb-In alloy.

The electrodes to which the bumps 3 of low melting point metal balls are adhesive bonded can be formed from an electrode material of Cu or a Cu alloy, Al or an Al alloy, or Au or a Au alloy. In the semiconductor device of the present invention, an electrode having a surface area of 900 to 22,500 μm^2 is preferably used. That is, when a square electrode is used, one of the sides of the electrode has a dimension of 30 to 150 μm.

When the electrode material is Al or an Al alloy, connecting solder balls (the term solder balls designates low melting metal balls hereinafter and is used below) to an electrode by reflowing deteriorates the bonding between the solder balls and the electrode. When Al or an Al alloy is used as an electrode material, at least one layer of a metal or an alloy of the metal having a melting point higher than the electrode material is laminated to the layer formed of the electrode material to avoid the deterioration. A typical example of the material used as the material therefor is a metal selected from Ti, W, Ni, Cr, Au, Pd, Cu, Pt, Ag, Sn and Pb, or an alloy of these metals. Of these substances, Ti, W, Ni, Cr, Pd, Cu or Pt, or an alloy of these metals is particularly effective in bonding between the material and the layer formed from Al or its alloy. Accordingly, any of the above metals or an alloy of these metals is preferably used as a layer contacted with the layer of Al or its alloy. Moreover, a solder generally shows good wettability with Ni, Au, Pd, Cu, Pt, Ag, Sn or Pb, or an alloy of these metals. Of layers laminated to the electrode material layer of Al or an Al alloy, the layer contacted with the solder ball is, therefore, preferably formed from these materials.

As explained above, when Al or an Al alloy is used, the electrode has a multilayered structure as illustrated in Fig. 2. In Fig. 2, an electrode 8 is formed as a laminated structure including a first layer 5 made of Al (or an Al alloy) on a surface of a semiconductor chip 2, a

second layer 6 made of Cr on the first layer, and a third layer 7 made of Cu on the second layer.

In addition to the laminated structure successively having from the semiconductor chip side an Al (or Al alloy) layer, a Cr layer and a Cu layer (such a laminated structure being represented as Al/Cr/Cu hereinafter) as illustrated in Fig. 2, examples of the laminated structure of the electrode in which Al or its alloy is used as an electrode material may include Al/Ni, Al/Ni/Au, Al/Ni/Cu/Au, Al/Cr/Cu/Au, Al/Ti/Cu/Au, Al/Ti/TiW (alloy)/Cu/Au, Al/TiW (alloy)/Cu/Au, Al/Cr/Ni/Pd, Al/Pd/Au, Al/Ni/Sn, Al/Cr/Cu/Pd and Al/Cr/Pt. It is needless to say that effective electrode laminated structures are not limited to the structures mentioned above in the semiconductor device of the present invention.

A flux is preferably used for adhesive bonding the solder ball to the electrode. Any of the fluxes generally used in producing semiconductor devices may be used. Although the flux may be applied to either the solder ball or the electrode surface, it is preferably applied to the electrode surface. Standard methods such as screen printing may be utilized for the method for applying the flux to the electrode surface.

When the semiconductor device of the present invention is flip chip bonded to a substrate, the solder ball bumps may be made to face the respective electrode terminals of the substrate, positioned, and contacted therewith, followed by reflowing the bumps. Such a procedure of flip chip bonding has been widely known, and it is needless to explain in detail.

The semiconductor device of the present invention may be flip chip bonded to the substrate after the solder balls are reflowed once to form semispherical bumps. Fig. 3 shows an example of a semispherical bump. The semispherical bump 10 in Fig. 3 is formed by reflowing the

solder ball bump 3 adhesive bonded to the laminated electrode 8 having been explained in Fig. 2.

In addition, the bump 10 in Fig. 3 formed by reflowing a solder ball is herein described as semispherical. The term is mainly based on the longitudinal sectional shape of the bump subsequent to reflowing as shown in Fig. 3. Electrodes on semiconductor chips have various shapes such as a circular shape, a square shape and other arbitrary shapes. For example, a bump formed by reflowing a solder ball on a square electrode has a semispherical longitudinal sectional shape as seen in Fig. 3. However, since the molten solder wets the entire square electrode surface and then solidifies, the shape viewed from above (transverse sectional shape) is not a circle but a square or a shape close to a square. Accordingly, it should be noted that the semispherical bump herein termed includes not only a bump appearing to have a circular cross sectional shape when viewed from above after reflowing but also a bump having an arbitrary transverse cross sectional shape reflecting the electrode shape under the bump. That is, "a semispherical bump" herein designates all sorts of bumps formed by reflowing solder balls adhesive bonded to electrodes having an arbitrary shape.

In order to appropriately form a semispherical bump on an electrode by reflowing a solder ball, the radius R of the solder ball to be adhesive bonded to the electrode is desirably selected so that the equation

$$0.4\sqrt{A} \leq R \leq 2\sqrt{A}$$

wherein A is the surface area of the electrode, is satisfied. When the radius R of the solder ball is less than $0.4\sqrt{A}$, the amount of the solder becomes insufficient, and formation of a good semispherical bump subsequent to reflowing becomes difficult. When the radius R of the solder ball exceeds $2\sqrt{A}$, the semispherical bump becomes large compared with the size of the electrode. Consequently, the bonded portion between the electrode and

the bump is subjected to stress concentration, and tends to be fractured.

When an electrode having a surface area of 900 to 22,500 μm^2 is used in the semiconductor device of the present invention, a preferred radius R of the solder ball derived from the above equation is from 12 to 300 μm.

An example of the production of a semiconductor device in the present invention will be explained by making reference to Fig. 4.

As shown in Fig. 4A, a 100 x 100 μm electrode 42 1.0 μm thick of an Al alloy (Al-Si-Cu alloy) is formed on a semiconductor chip 41 by sputtering. The reference numeral 43 in the figure designates a passivation film which compartments the electrode thus formed. Next, a metal layer 44 of Ni and a metal layer 45 of Cu each having a thickness of 80 nm are successively laminated to the chip electrode 42 by sputtering, as shown in Fig. 4B.

What is explained above is about the step for forming a substrate on which a low melting point metal bump is to be formed. Next, as shown in Fig. 4C, a solder ball 46 of Pb-Sn alloy having a diameter of 80 μm is adhesive bonded to the Cu metal layer 45. At the time of adhesive bonding the solder ball, the surface of the metal layer 45 is first coated with a flux (not shown) by screen printing. In cases where, for example, the solder ball placed on the electrode is subsequently to be reflowed in a reducing atmosphere, coating the metal layer 45 with the flux may be omitted. The solder ball 46 is then adhesive bonded to the flux. A preferred method for adhesive bonding the solder ball to the electrode will be explained later.

The semiconductor device of the present invention thus prepared can be flip chip bonded to a substrate by making the solder ball bumps face the respective corresponding electrode terminals of the substrate, positioning the bumps, contacting the bumps with the respective electrode terminals thereof, and reflowing the bumps.

The semiconductor device of the present invention provided with the bumps of solder balls 46 as shown in Fig. 4C may also be flip chip bonded to the substrate after forming semispherical bumps 47 by reflowing the solder balls once as shown in Fig. 4D.

Since an Al alloy is used as an electrode material in the above example, the Ni layer and the Cu layer are laminated to the Al alloy layer so as to firmly bond the semiconductor device to the substrate by the solder bump. However, when the electrode material is neither Al nor Al alloy, for example, when the electrode material is Cu or a Cu alloy, or Au or a Au alloy, the substrate (one or more metal (or alloy) layers on the electrode material layer) for forming low melting point metal bumps is not required to be formed. Accordingly, as shown in Fig. 5, a bump of a solder ball 53 can be directly formed on an electrode 52 of a semiconductor chip 51. The solder ball bump may also be reflowed once to be formed into a semispherical bump, which is thereafter used for flip chip bonding.

Another example will now be described, in which solder ball bumps having a diameter of 150 μm are formed on an electrode having a diameter of 50 μm. In this case, Cr, Cu, and Au layers are successively superposed by sputtering process on an electrode of Al-Cu alloy having a diameter of 50 μm and a thickness of 1.0 μm, the superposed Cr, Cu, and Au layers having a thickness of 80 nm, 80 nm, and 30 nm, respectively, and a diameter which is the same as or somewhat larger than the diameter of the electrode. The surface of the Au layer is then coated with a flux, on which a solder ball of Pb-Sn alloy having a diameter of 150 μm is adhesive bonded. Shear test carried out for semispherical bumps formed by reflowing the solder balls revealed that all fractures occurred in the solder balls, and no fracture was observed at the bonded portions between the bumps and electrodes.

Next, a preferred method for adhesive bonding the solder balls to the electrodes will be explained. At

present, an explanation will be made of adhesive bonding the solder balls to not electrodes each having a multilayered structure but electrodes each composed of a single material as explained in Fig. 5.

As shown in Fig. 6A, a vibration at a small amplitude is applied to a vessel 60 containing the solder balls 53 to cause the solder balls 53 to jump up. The solder balls 53 are then arranged and held on an arrangement base plate 63 by attracting the jumping up solder balls 53 to attraction openings 61 (attracting mechanism for attracting the solder balls being not shown) provided in the arrangement base plate 63 in positions corresponding to positions of the electrodes of the semiconductor chip to which the solder balls 53 are to be adhesive bonded. During attracting and arranging the solder balls, excess solder balls 53' adhere to portions of the arrangement base plate 63 other than the attraction openings 61, or other excess solder balls 53" adhere to the solder balls 53 attracted to the attraction openings 61, as shown in Fig. 6A. The excess solder balls 53', 53" are, therefore, removed. To achieve the removal, arbitrary procedures may be utilized. For example, excess solder balls 53', 53" can be preferably removed by applying an ultrasonic vibration to the arrangement base plate 63 in the horizontal direction. Although only two attraction openings 61 are shown in the attraction base plate 63 in Fig. 6A for the sake of simplicity, it should be noted that the actual arrangement base plate has the attraction openings the number of which is the same as that of the solder balls to be adhesive bonded to the electrodes of the semiconductor chip.

Next, as shown in Fig. 6B, the arrangement base plate 63 holding the solder balls 53 in predetermined positions is moved above the semiconductor chip 51 so that the solder balls 53 are properly positioned with respect to the respective electrodes 52 of the semiconductor chip 51. The arrangement base plate 63 is then moved downward so

that the solder balls 53 are contacted with the respective electrodes 52. After the contact, attracting the solder balls 53 to the arrangement base plate 63 is stopped (by stopping the attraction mechanism), and the arrangement base plate 63 is moved upward.

When the surface of the electrodes 52 is coated with a flux (not shown in the figure), the solder balls 53 are adhesive bonded to the electrodes due to the adhesion thereof. When the surface of the electrodes 52 is not coated with a flux, semispherical bumps adhesive bonded to the respective electrodes 52 can be formed by, for example, reflowing the solder balls 53 in a reducing atmosphere, as referred to above.

Since solder bumps can simultaneously be adhesive bonded to a large number of the respective electrodes of a semiconductor chip by the process as explained above, the process is very advantageous to the production of the semiconductor device of the present invention.

In general, a large number of semiconductor chips are formed on one wafer, and separated by cutting to give individual chips. The process as mentioned above may also be applied to a plurality of semiconductor chips prior to separation of them from the wafer by cutting, or it may be applied to individual semiconductor chips subsequently to separation of them therefrom. It is evident from what has been explained above that the semiconductor chip in the present invention includes not only a separated individual semiconductor chip but also a plurality of semiconductor chips in a state of being produced on one wafer.

It is evident from what has been explained above that the semiconductor device of the present invention is provided with low melting point metal ball bumps directly adhesive bonded to the respective electrodes formed on a semiconductor chip. The bumps can be made of high quality by making the size of the metal balls uniform. The metal balls are not formed on the electrodes of the semiconductor chip by a procedure such as plating or vapor

deposition in conventional processes, but can be adhesive bonded to the electrodes. Accordingly, the semiconductor device of the present invention can be produced without a mask, and without fear of environmental pollution.

Furthermore, the amount of bumps can be easily and highly accurately controlled by adjusting the size of the low melting point metal balls, to enhance reliability of bumps.

Industrial Applicability

The present invention can be advantageously applied to flip chip bonding which makes possible high density mounting of a semiconductor device on a substrate.

CLAIMS

1. A semiconductor device comprising electrodes formed on a semiconductor chip, and bumps each consisting of a spherically formed low melting point metal ball having a given size, and adhesive bonded to the electrodes.

2. The semiconductor device according to claim 1, wherein the low melting metal balls are adhesive bonded to the electrodes with a flux.

3. The semiconductor device according to claim 1 or 2, wherein the electrodes are formed from an electrode material of Cu or a Cu alloy, Al or an Al alloy, or Au or a Au alloy.

4. The semiconductor device according to claim 3, wherein the electrodes each comprise a layer of an electrode material composed of Al or an Al alloy, and at least one metal layer or metal alloy layer laminated to the electrode material layer and having a melting point higher than the electrode material.

5. The semiconductor device according to claim 4, wherein the at least one layer laminated to the electrode material layer is formed from a metal selected from Ti, W, Ni, Cr, Au, Pd, Cu, Pt, Ag, Sn or Pb or an alloy of these metals.

6. The semiconductor device according to claim 5, wherein the at least one layer laminated to the electrode material and contacted with the electrode material layer is formed from Ti, W, Ni, Cr, Pd, Cu or Pt, or an alloy of these metals, and the at least one layer farthest from the electrode material layer contacted with the low melting point metal ball is formed from Ni, Au, Pd, Cu, Pt, Ag, Sn or Pb, or an alloy of these metals.

7. A process for producing a semiconductor device comprising electrodes formed on a semiconductor chip, and bumps each consisting of a low melting point metal ball spherically formed, having a given size and adhesive bonded to the electrodes, the process comprising adhesive

bonding the low melting point metal balls to the electrodes with a flux.

8. The process according to claim 7, wherein the flux is applied to the electrodes.

9. The process according to claim 7 or 8, wherein the low melting point metal balls are adhesive bonded to the electrodes by a process comprising the steps of:

applying a vibration at a small amplitude to a vessel containing the low melting point metal balls to cause the low melting point metal balls to jump up;

arranging and holding the low melting point metal balls on an arrangement base plate by attracting the jumping up low melting point metal balls to attraction openings provided in the arrangement base plate in positions corresponding to the electrodes of the semiconductor chip to which the low melting point metal balls are to be adhesive bonded;

removing excess low melting point metal balls adhering either to the arrangement base plate or to the low melting point metal balls attracted to the attraction openings; and

simultaneously contacting the low melting point metal balls held and arranged on the arrangement base plate with the electrodes of the semiconductor chip.

10. A process for producing a semiconductor device provided with low melting point metal bumps on a semiconductor chip, the process comprising the steps of:

adhesive bonding low melting point metal balls each being spherically formed and having a given size to the electrodes, and

reflowing the low melting point metal balls.

11. The process according to claim 10, wherein the low melting point metal balls are adhesive bonded to the respective electrodes with a flux.

12. The process according to claim 11, wherein the flux is applied to the electrodes.

13. The process according to any one of claims 10 to 12, wherein the low melting point metal balls are adhesive bonded to the electrodes by a process comprising the steps of:

applying a vibration at a small amplitude to a vessel containing the low melting point metal balls to cause the low melting point metal balls to jump up;

arranging and holding the low melting point metal balls on an arrangement base plate by attracting the jumping up low melting point metal balls to attraction openings provided in the arrangement base plate in positions corresponding to the electrodes of the semiconductor chip to which the low melting point metal balls are to be adhesive bonded;

removing excess low melting point metal balls adhering either to the arrangement base plate or to the low melting point metal balls attracted to the attraction openings; and

simultaneously contacting the low melting point metal balls held and arranged on the arrangement base plate with the electrodes of the semiconductor chip.

14. A semiconductor device produced by the process according to any one of claims 7 to 9, and provided with bumps consisting of low melting point metal balls and adhesive bonded to the respective electrodes of a semiconductor chip.

15. A semiconductor device produced by the process according to any one of claims 10 to 13, and provided with bumps consisting of low melting point metal on the electrodes of a semiconductor chip.

ABSTRACT

A semiconductor device (1) comprising electrodes formed on a semiconductor chip (2) and bumps (3) which consist of a low melting point metal ball spherically formed and having a given size and which are adhesive bonded to the electrodes (5). The electrodes (5) are formed from an electrode material of Cu or a Cu alloy, Al or an Al alloy, or Au or a Au alloy. When the electrode material is composed of Al or an Al alloy, the electrodes contain, on the electrode material layer of Al or an Al alloy, at least one layer (6) composed of a metal or metal alloy (preferably a metal selected form Ti, W, Ni, Cr, Au, Pd, Cu, Pt, Ag, Sn or Pb, or an alloy of these metals) having a melting point higher than the electrode material. The low melting point metal balls (3) are adhesive bonded to the electrodes (5) preferably with a flux. The low melting point metal balls (3) adhesive bonded to the respective electrodes (3) may also be reflowed to form semispherical bumps (10) before use.

Fig.1

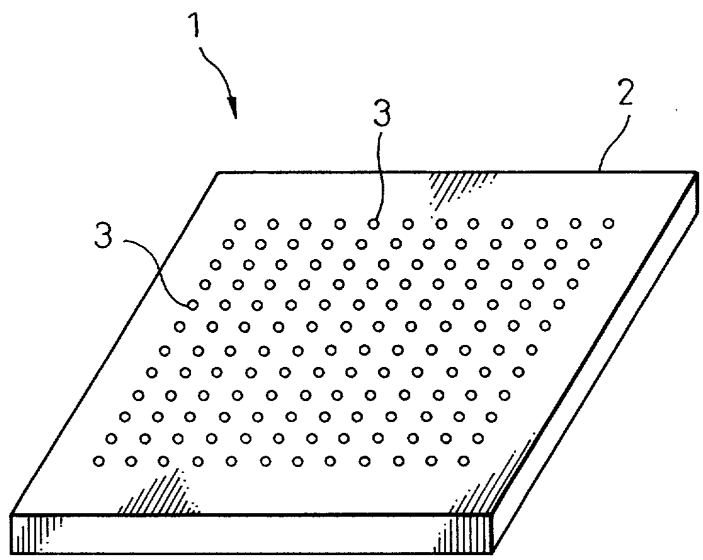


Fig. 2

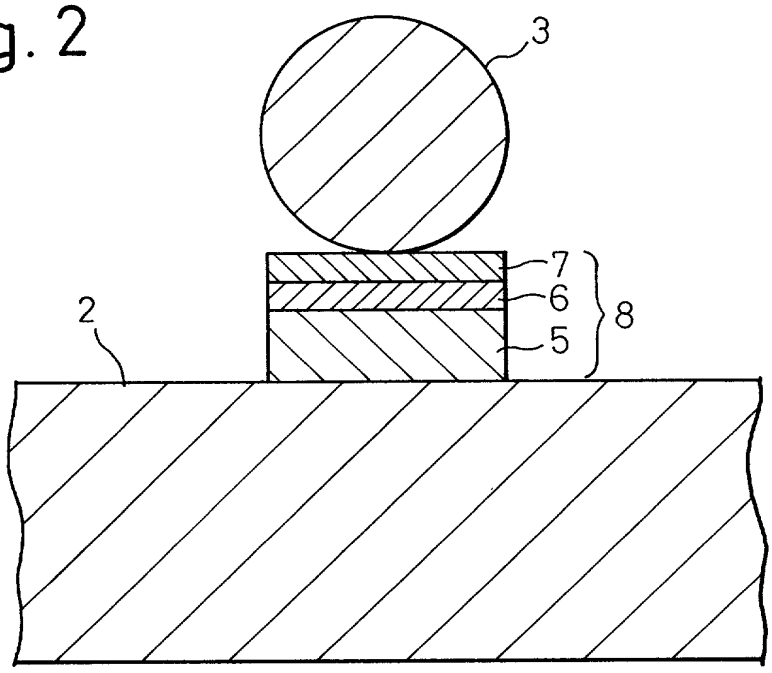


Fig. 3

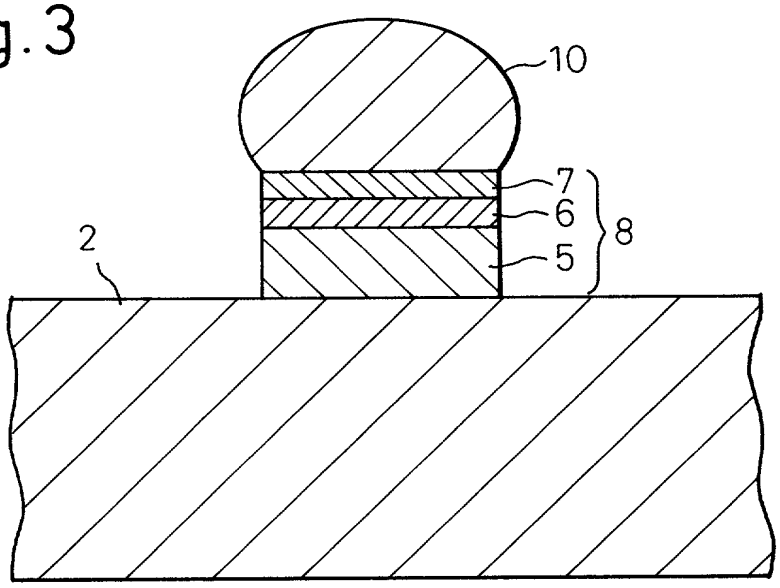


Fig. 4A

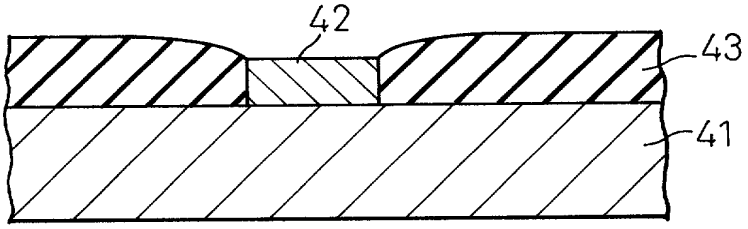


Fig. 4B

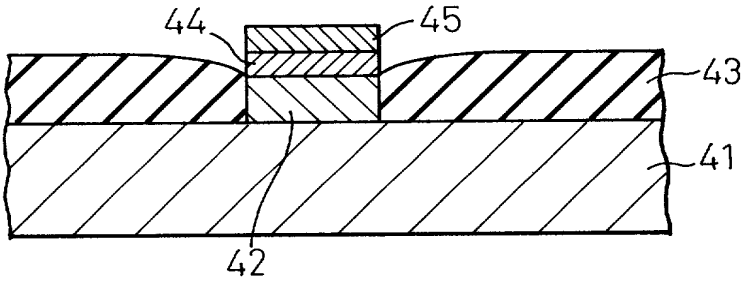


Fig. 4C

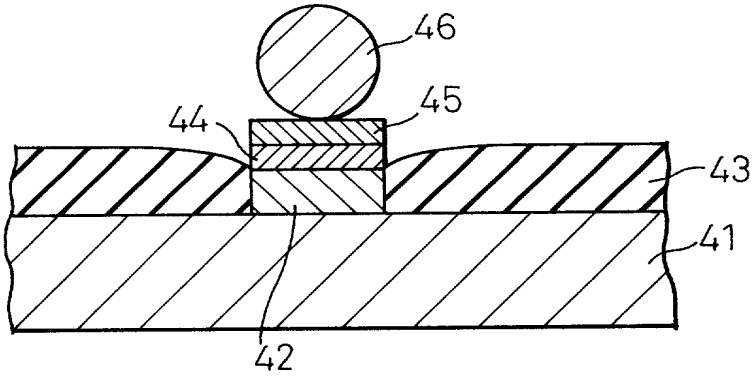


Fig. 4D

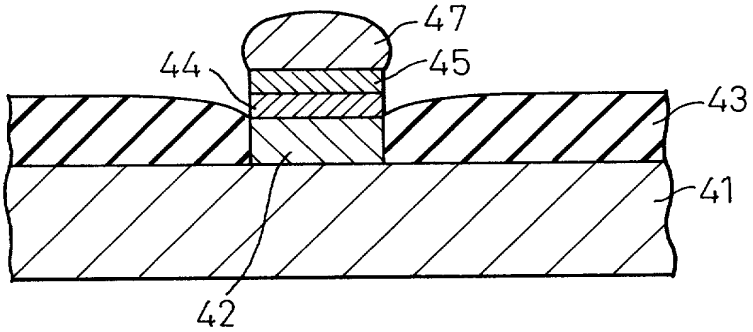


Fig.5

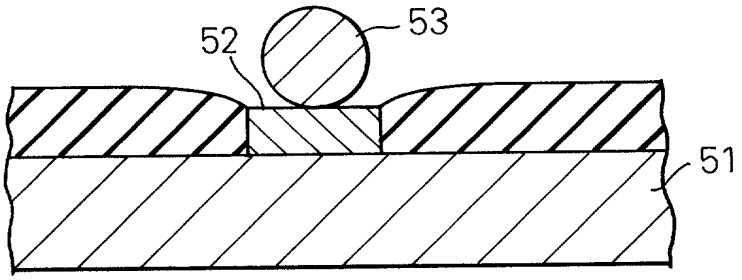


Fig.6A

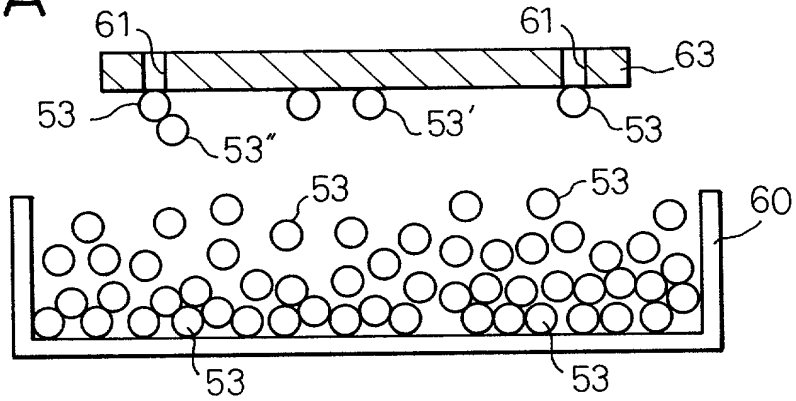
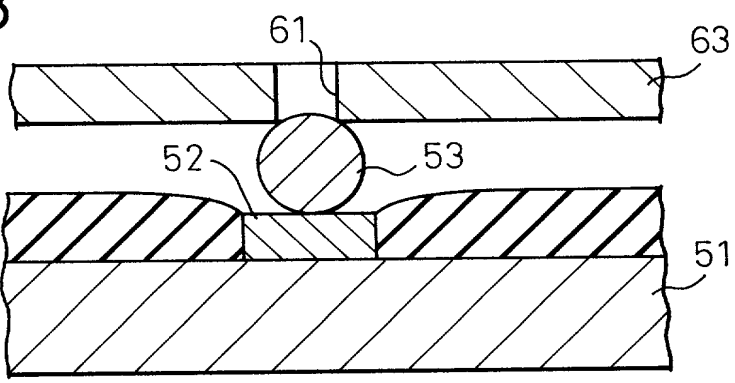


Fig.6B



Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR DEVICE PROVIDED WITH LOW MELTING POINT METAL BUMPS AND PROCESS FOR PRODUCING SAME

上記発明の明細書（下記の欄でx印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
（該当する場合）_____ に訂正されました。

☒ was filed on August 27, 1997
as United States Application Number or
PCT International Application Number
PCT/JP97/02987
and was amended on
_____
(if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

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私は、米国法典第３５編１１９条(a)-(d)項又は３６５条(b)項に基き下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約３６５(a)項に基ずく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、印内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) 外国での先行出願			Priority Not Claimed 優先権主張なし
8-244269(Pat.Appln.) (Number) (番号)	Japan (Country) (国名)	27/August/1996 (Day/Month/Year Filed) (出願年月日)	□
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	□

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(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

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(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Approved for use through 9/30/98 OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Japanese Language Declaration
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委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*

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第六共同発明者	日付	Sixth inventor's signature Date
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（第七以降の共同発明者についても同様に記載し、署名をすること）

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